S/N 09/608,580 PATENT

AMENDMENT UNDER 37 C.F.R. §1.116-- EXPEDITED EXAMINATION PROCEDURE

#7/B (INP) marsha 7/23/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Frankie F. Roohparvar	Examiner:	Trong Q. Phan
Serial No.:	09/608,580	Group Art Unit:	2818
Filed:	June 30, 2000	Docket:	400.006US01
Title:	ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY		

AMENDMENT AND RESPONSE UNDER 35 U.S.C. § 1.116

Commissioner for Patents
BOX AF
Washington, D.C. 20231

In response to the Final Office Action mailed May 15, 2002, please consider the following remarks:

Please amend the application as follows:

Do not enter TP 7/23/02

IN THE CLAIMS

Please amend the claims as rewritten below:

16. The synchronous memory device of claim 15 wherein the memory array is arranged in a plurality of memory blocks, and the control circuitry is configured to copy the data from the write latch to a first block of the plurality of memory blocks.

25. The memory system of claim 24 wherein the memory array is arranged in a plurality of memory blocks, and the synchronous memory comprises control circuitry configured to copy the data from the write latch to a first block of the plurality of memory blocks.